REMARKS

Claims 1-35 were examined and reported in the Office Action. Claims 1-35 are rejected. Claim 8 is canceled. Claims 1, 4, 9, 11, 14-15, 17, 20, 29 and 32 are amended. Claims 1-7 and 9-35 remain.

Applicant requests reconsideration of the application in view of the following remarks.

I. Drawings

The drawings are objected to because they do not show every feature of the invention specified in the claims and other informalities. Figure 7 has been corrected. Figure 5 is amended. Figures 8 and 9 are added. The integer register buffer and predicate register buffer illustrated in Figure 8 are disclosed in the original specification, paragraph [0014]. The process illustrated in Figure 9 is disclosed in the original specification, paragraph [0029]. Therefore, no new matter is added. Applicant submits all drawings including the aforementioned amended drawings as a formal drawing submission. Approval is respectfully requested.

II. Specification Objections

It is asserted in the Office Action that the specification is objected to as it is not clear how to spawn the speculative thread and how value prediction is implemented. Applicant asserts that paragraph [0016] asserts that "... program execution begins as a single thread on one of commit CPU 110 and speculative CPU 120. In one embodiment of the invention, commit CPU 110 fetches, decodes, executes and updates register file 212, as well as issue load instructions/commands (loads) and stores to memory as instructed by the program. As the instructions are decoded, commit CPU 110 may direct speculative CPU 120 to start executing a speculative thread at some program counter value. This program counter value may be the address of the next instruction in memory, or it may be supplied as a hint by a compiler. For example, a fork at a next

instruction address may be a thread forked at a call instruction. Speculative CPU 120 continues its thread execution until a program counter in commit CPU 110 reaches the same point in the program execution for which the speculative thread program counter points. Therefore, commit CPU 110 fetches, issues and commits every instruction in the program, even when an instruction belongs to a speculative thread." Regarding how value prediction is implemented, paragraph [0020] asserts that "[d]epending on the data flow in a particular program, commit CPU 110 may produce some register or memory input values after these inputs are read by the speculative thread. In one embodiment of the invention, to relax the limitations imposed by register and memory data flow, value prediction is used to provide initial input values to the speculative thread. In one embodiment of the invention, a simple value prediction method is used having passive prediction. In this embodiment, it is assumed that register and memory input values have already been produced by commit CPU 110 at the time the speculative thread is spawned."

Applicant notes that value prediction is well known in the art. The basic idea of value prediction is to have the processor guess what value will be returned by a load instruction, and have it compute speculatively with this value. When the load completes, the actual value returned by the memory system is compared with the guess; if the guess is correct, the processor simply notes that fact and continues, but if the guess is incorrect, the processor rolls back the computation and recomputes with the actual value. Simple value prediction can just guess "0."

Regarding the objection to paragraph 26, Applicant notes that paragraph 12 asserts that the load buffer is coupled to both commit and speculative processor; paragraphs 25-26 assert the speculative processor posts loads in the load buffer; and paragraph 31 asserts the commit processor issues loads to the load buffer. Therefore, Applicant respectfully asserts that it is clear that both processors can post to the load buffer.

Regarding the assertion in the Office Action that "the 'store valid bit' is in both the store buffer and the load buffer, Applicant respectfully traverses. Applicant notes

that in paragraph 28 it is asserted that the store valid bit is in the load buffer and is not illustrated. Applicant notes that store buffer valid portion 430 and entry valid bit 530 are not the store valid bit.

Regarding the query as to what replayed instructions are, it is very well known in the art that replayed instructions are instructions that must be re-executed. Both processors replay instructions if necessary. The speculative processor allows speculative multithreading when executing single-threaded applications with selective recovery, aggressive far-ahead pre-fetch and execution on a single chip multiprocessor. Note that stores also access the load buffer. An address matching store that also matches the store ID sets the load entry valid bit. A store later in the pipeline that hits an entry invalidates the entry. When a store invalidates an entry, the entry load ID is used to index the trace buffer to set the mispredicted load bit. When a load is fetched and the mispredicted bit in the trace buffer is found to be set, the load destination register scoreboard bit is set. This optimization reduces the number of flushes that occur as a result of load misses in the load buffer. Note that the commit processor concurrently reads the trace buffer and the instruction cache. This enables setting the scoreboard bit for a mispredicted load in time without creating a bubble in the pipeline.

Regarding the query in paragraph D on page four of the Office Action, speculative results are found to be correct if no replay results and no mispredictions occur.

Regarding the query in paragraph E on page four of the Office Action, Applicant notes that paragraph 16 in the specification asserts "As the instructions are decoded, commit CPU 110 may direct speculative CPU 120 to start executing a speculative thread at some program counter value." The replay mode concerns the speculative thread. (See Applicant's specification, paragraph 33).

The headings are amended to remove the underlining.

It is asserted in the Office Action that the specification is objected to for failing to provide antecedent basis. Applicant respectfully traverses. In Claim 16, the limitations

set forth are "flushing a pipeline, setting a mispredicted bit in a load entry in the trace buffer and restarting a load instruction **if one of** the load is not replayed and does not match a tag portion in a load buffer, and the load instruction matches the tag portion in the load buffer while a store valid bit is not set. This limitation has the same meaning if the grammar were to be: flushing a pipeline, setting a mispredicted bit in a load entry in the trace buffer and restarting a load instruction **if** the load is not replayed and does not match a tag portion in a load buffer **or** the load instruction matches the tag portion in the load buffer while a store valid bit is not set. The language in paragraph 29 asserts "In one embodiment of the invention, upon a clean (not replayed) load not matching any tag 520, **or** a load matching tag 520 with the store valid bit clear (set to "0"), the pipeline is flushed, the mispredicted bit in the load entry in trace buffer 140 is set to one ("1"), and the load instruction is restarted." Further, in paragraph 28, it is asserted that "In load buffer 150 (illustrated in **Figure 5**) each entry 510 comprises a tag portion 520." Therefore, there is antecedent basis for the limitation "the tag portion in the load buffer." Note that Applicant amends paragraph 29 to add the term "portion" after "tag."

III. Claim Objections

It is asserted in the Office Action that claim 4 and 32 are objected to because of informalities. Applicant has amended claims 4 and 32 to overcome the informal objections.

Accordingly, withdrawal of the Examiner's objections for claims 4 and 32 is respectfully requested.

IV. 35 U.S.C. §112, first paragraph

A. It is asserted in the Office Action that claim 14, 15 and 18 are rejected under 35 U.S.C. §112, first paragraph, as based on a disclosure which is not enabling. Applicant respectfully traverses the aforementioned rejection for the following reasons.

It is asserted in the Office Action that "knowing what a replayed instruction is and in which processor it is executed in is critical or essential to the practice of the invention." Applicant submits that an ordinary person skilled in the art would know what a replayed instruction is. All one would have to do is a quick Internet search or search of the U.S.P.T.O. database using terms similar to ""replay instruction" AND processor." Then look to any found material that predates Applicant's filing date. In plain English, replayed is defined as "to play again or over." (Merriam-Webster Online Dictionary, http://www.m-w.com/cgi-bin/dictionary?book=Dictionary&va=replayed." Therefore, a replayed instruction is simply an instruction that is resubmitted in the pipeline. As far as which processor executes a replayed instruction, either processor can execute a replayed instruction. Regarding how to know which store ID portion to compare with, Applicant has amended claims 14 and 15 by adding the limitations "in a load buffer."

Therefore, since a person of ordinary skill in the art of processor instruction scheduling would know what a replayed instruction is, the limitation of "replayed instruction" is not critical or essential to the practice of Applicant's invention. And, replayed instructions can be executed in any pipeline, i.e. either processor.

Accordingly, withdrawal of the 35 U.S.C. §112, first paragraph rejections for claims 14, 15 and 18 are respectfully requested.

B. It is asserted in the Office Action that claim 16 is rejected under 35 U.S.C. §112, first paragraph, as based on a disclosure which is not enabling. Applicant respectfully traverses the aforementioned rejection for the following reasons.

Applicant asserts that the limitations "if one of the load is not replayed and does not match a tag portion in a load buffer, and the load instruction matches the tag portion in the load buffer while a store valid bit is not set" has the following interpretation: "if ~~one of~~ [the load is not replayed and does not match a tag portion in a load buffer]~~, and~~ **OR** [the load instruction matches the tag portion in the load buffer

while a store valid bit is not set]." The terms "one of A, and B is interpreted as either A or B.

Regarding knowing which load to be checked, one skilled in the art would know that each load in a pipeline is compared.

Accordingly, withdrawal of the 35 U.S.C. §112, first paragraph rejections for claim 16 is respectfully requested.

V. 35 U.S.C. §112, second paragraph

It is asserted in the Office Action that claims 16 and 17 are rejected under 35 U.S.C. §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Applicant respectfully traverses the aforementioned rejection for the following reasons.

Regarding claim 16, it is asserted in the Office Action that the term "one of the load" refers to one of a plurality of load instructions. Applicant respectfully disagrees. It is well known that the alternative claim language of one of A, and B is interpreted as follows: either A or B. Therefore, the limitations of claim 16 are interpreted as asserted in section III above.

Regarding claim 17, Applicant has amended claim 17 to overcome the 35 U.S.C. §112, second paragraph rejection.

Accordingly, withdrawal of the 35 U.S.C. §112, second paragraph rejections for claims 16-17 are respectfully requested.

VI. 35 U.S.C. §102(a)

It is asserted in the Office Action that claims 1-7, 11-13, 17, 19 are rejected under 35 U.S.C. §102(a) as being anticipated by Sundaramoorthy et al. ("Slipstream Processors: Improving both Performance and Fault Tolerance", ASPLOS, pp. 257-268, Nov. 2000)

("Sundaramoorthy"). Applicant respectfully traverses the aforementioned rejections for the following reasons.

According to MPEP §2131, "'[a] claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference.' (Verdegaal Bros. v. Union Oil Co. of California, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987)). 'The identical invention must be shown in as complete detail as is contained in the ... claim.' (Richardson v. Suzuki Motor Co., 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989)). The elements must be arranged as required by the claim, but this is not an ipsissimis verbis test, i.e., identity of terminology is not required. (In re Bond, 910 F.2d 831, 15 USPQ2d 1566 (Fed. Cir. 1990))."

Applicant's claim 1 contains the limitations of "[a] apparatus comprising: a first processor and a second processor each having a scoreboard and a decoder; a plurality of memory devices coupled to the first processor and the second processor; a register buffer coupled to the first processor and the second processor; a trace buffer coupled to the first processor and the second processor; and a plurality of memory instruction buffers coupled to the first processor and the second processor; wherein the first processor and the second processor perform single threaded applications using multithreading resources."

Applicant's claim 11 contains the limitations of "[a] method comprising: executing a plurality of instructions in a first thread by a first processor; executing the plurality of instructions in the first thread by a second processor as directed by the first processor, the second processor executing the plurality of instructions ahead of the first processor; and tracking at least one register that is one of loaded from a register file buffer, and written by said second processor, said tracking executed by said second processor."

Sundaramoorthy discloses a multiprocessor system that executes redundant programs on separate processors on the same chip. The redundant programs, however,

have different amount of instructions. That is, one of the programs has more instructions than the other. And, both programs run in parallel on two processors. Sundaramoorthy, however, does not teach, disclose or suggest the limitations in claim 1 of "a first processor and a second processor each having a scoreboard and a decoder," nor the limitations of claim 11 of "tracking at least one register that is one of loaded from a register file buffer, and written by said second processor, said tracking executed by said second processor."

Therefore, since Sundaramoorthy does not disclose, teach or suggest all of Applicant's amended claims 1 and 11 limitations, Applicant respectfully asserts that a *prima facie* rejection under 35 U.S.C. § 102(a) has not been adequately set forth relative to Sundaramoorthy. Thus, Applicant's amended claims 1 and 11 are not anticipated by Sundaramoorthy. Additionally, the claims that directly or indirectly depend on claims 1 and 11, namely claims 2-7, and 12-13, 17 and 19, respectively, are also not anticipated by Sundaramoorthy for the same reason.

Accordingly, withdrawal of the 35 U.S.C. §102(a) rejections for claims 1-7, 11-13, 17 and 19 are respectfully requested.

VII. 35 U.S.C. §103

A. It is asserted in the Office Action that claims 8-10 are rejected under 35 U.S.C. §103(a) as being unpatentable over Sundaramoorthy in view of no other prior art. Applicant believes there is a typographical error in the Office Action and assumes it was meant to reject claims 7 and 9-10. Applicant respectfully traverses the aforementioned rejections for the following reasons.

According to MPEP §2142 "[t]o establish a prima facie case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The

teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure." (In re Vaeck, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991)). Further, according to MPEP §2143.03, "[t]o establish prima facie obviousness of a claimed invention, all the claim limitations must be taught or suggested by the prior art. (In re Royka, 490 F.2d 981, 180 USPQ 580 (CCPA 1974)." *"All words in a claim must be considered* in judging the patentability of that claim against the prior art." (In re Wilson, 424 F.2d 1382, 1385, 165 USPQ 494, 496 (CCPA 1970), emphasis added.)

Applicant's claim 7and 9-10 directly depend on amended claim 1 (claim 8 is canceled). As asserted above in section VI, Sundaramoorthy does not teach, disclose or suggest the limitations contained in claim 1 of "a first processor and a second processor each having a scoreboard and a decoder."

Further, it is asserted in the Office Action that structure of the load ordering buffer is nonfunctional descriptive material and not involved in the functioning of the load ordering buffer. Applicant respectfully traverses this opinion as the structure of the load ordering buffer cannot help but to be critical in the functioning of the load ordering buffer. That is, without the specifically claimed structure the load ordering buffer would be useless to the claimed invention.

Similarly, it is asserted in the Office Action that structure of the register buffer is nonfunctional descriptive material and not involved in the functioning of the register buffer. Applicant respectfully traverses this opinion as the structure of the register buffer cannot help but to be critical in the functioning of the register buffer. That is, without the specifically claimed structure the register buffer would be useless to the claimed invention.

Sundaramoorthy does not teach, disclose or suggest the limitations contained in Applicant's amended claim 1, as listed above. Since Sundaramoorthy does not teach, disclose or suggest all the limitations of Applicant's amended claim 1, there would not be any motivation to arrive at Applicant's claimed invention. Thus, Applicant's

amended claim 1 is not obvious over Sundaramoorthy in view of no other prior art since a *prima facie* case of obviousness has not been met under MPEP §2142. Additionally, the claims that directly or indirectly depend from amended claim 1, namely claims 7 and 9-10 (claim 8 is canceled), would also not be obvious over Sundaramoorthy in view of no other prior art for the same reason.

Accordingly, withdrawal of the 35 U.S.C. § 103(a) rejections for Claims 7 and 9-10 are respectfully requested.

B. It is asserted in the Office Action that claims 14-16 are rejected under 35 U.S.C. §103(a) as being unpatentable over Sundaramoorthy in view of Akkary (WO 99/31594). Applicant respectfully traverses the aforementioned rejection for the following reasons.

Applicant's claims 14-16 indirectly depend on amended claim 11. As asserted above in section VI, Sundaramoorthy does not teach, disclose or suggest the limitations contained in Applicant's amended claim 11 of "tracking at least one register that is one of loaded from a register file buffer, and written by said second processor, said tracking executed by said second processor."

It is asserted in the Office Action that Official Notice is taken that it is well known and expected to set a status bit to indicate the change of state. Applicant agrees. However, how a state is changed and which specific bits are set in order to effect actions is not well known or expected, and much narrower than the broad limitation of setting of a status bit to indicate state. Therefore, Applicant respectfully traverses the Official Notice.

It is asserted in the Office Action that one would be motivated to modify Sundaramoorthy by clearing a store validity bit and setting a mispredicted bit in a load entry in a trace buffer if a replayed store instruction has a matching store ID portion because "the Sundaramoorthy reference does not provide enough detail on how to handle loads and stores..." Applicant respectfully asserts that one would not and could not be motivated to modify a known system by guessing that the Akkary disclosure

would make sense to be added. A similar statement can be made that by adding the disclosure of Akkary to Sundaramoorthy would render Sundaramoorthy useless.

Moreover, by viewing the disclosures of Sundaramoorthy and Akkary, one can not jump to the conclusion of obviousness without impermissible hindsight. According to MPEP 2142, [t]o reach a proper determination under 35 U.S.C. 103, the examiner must step backward in time and into the shoes worn by the hypothetical 'person of ordinary skill in the art' when the invention was unknown and just before it was made. In view of all factual information, the examiner must then make a determination whether the claimed invention 'as a whole' would have been obvious at that time to that person. Knowledge of applicant's disclosure must be put aside in reaching this determination, yet kept in mind in order to determine the 'differences,' conduct the search and evaluate the 'subject matter as a whole' of the invention. The tendency to resort to 'hindsight' based upon applicant's disclosure is often difficult to avoid due to the very nature of the examination process. However, impermissible hindsight must be avoided and the legal conclusion must be reached on the basis of the facts gleaned from the prior art." Applicant submits that without first reviewing Applicant's disclosure, no thought, whatsoever, would have been made to clearing a store validity bit and setting a mispredicted bit in a load entry in a trace buffer if a replayed store instruction has a matching store ID portion, or "tracking at least one register that is one of loaded from a register file buffer, and written by said second processor, said tracking executed by said second processor."

Neither Sundaramoorthy, Akkary, nor the combination of the two, teach, disclose or suggest the limitations contained in Applicant's amended claim 11, as listed above. Since neither Sundaramoorthy, Akkary, nor the combination of the two, teach, disclose or suggest all the limitations of Applicant's amended claim 11, there would not be any motivation to arrive at Applicant's claimed invention. Thus, Applicant's amended claim 11 is not obvious over Sundaramoorthy in view of Akkary since a *prima facie* case of obviousness has not been met under MPEP §2142. Additionally, the claims that directly or indirectly depend from amended claim 11, namely claims 14-16, would also not be obvious over Sundaramoorthy in view of Akkary for the same reason.

Accordingly, withdrawal of the 35 U.S.C. § 103(a) rejections for Claims 14-16 are respectfully requested.

C. It is asserted in the Office Action that claim 18 is rejected under 35 U.S.C. §103(a) as being unpatentable over Sundaramoorthy in view of Hennessy and Patterson ("Computer Architecture A Quantitative Approach", Morgan Kaufmann, 1996) ("Hennessy and Patterson"). Applicant respectfully traverses the aforementioned rejections for the following reasons.

Applicant's claim 18 indirectly depends on amended claim 11. As asserted above in section VI, Sundaramoorthy does not teach, disclose or suggest the limitations of "tracking at least one register that is one of loaded from a register file buffer, and written by said second processor, said tracking executed by said second processor."

Hennessy and Patterson are relied upon for disclosing "register renaming is used to reduce name dependencies allowing instructions involved in name dependencies to execute simultaneously or be reordered." (Office Action, page 24, paragraph 82). Hennessy and Patterson does not teach, disclose or suggest "tracking at least one register that is one of loaded from a register file buffer, and written by said second processor, said tracking executed by said second processor."

Moreover, the reason Hennessy and Patterson are relied on is not consistent with Applicant's claim language. Applicant's claim 18 contains the limitations of "supplying names from the trace buffer to preclude register renaming." Merriam-Webster online dictionary defines the meaning of "preclude" as "to make impossible by necessary consequence : rule out in advance." Therefore, while Applicant is supplying names from the trace buffer, Applicant is doing so to not rename registers. Therefore, Applicant respectfully asserts the Hennessy and Patterson disclosure does not teach, disclose or suggest precluding register renaming.

Neither Sundaramoorthy, Hennessy and Patterson, nor the combination of the two, teach, disclose or suggest the limitations contained in Applicant's amended claim 11 and claim 18, as listed above. Since neither Sundaramoorthy, Hennessy and

Patterson, nor the combination of the two, teach, disclose or suggest all the limitations of Applicant's amended claim 11 and claim 18, there would not be any motivation to arrive at Applicant's claimed invention. Thus, Applicant's amended claim 11 and claim 18 are not obvious over Sundaramoorthy in view of Hennessy and Patterson since a *prima facie* case of obviousness has not been met under MPEP §2142.

Accordingly, withdrawal of the 35 U.S.C. § 103(a) rejections for Claim 18 is respectfully requested.

D. It is asserted in the Office Action that claims 20-22, 26, and 28 are rejected under 35 U.S.C. §103(a) as being unpatentable over Sundaramoorthy in view of Tannenbaum ("Structured Computer Organization," Prentice-Hall, 1984, pp. 10-12) ("Tannenbaum"). Applicant respectfully traverses the aforementioned rejections for the following reasons.

Applicant's amended claim 20 contains the limitations of "tracking at least one register that is one of loaded from a register file buffer, and written by said second processor, said tracking executed by said second processor." As asserted above in section VI, Sundaramoorthy does not disclose, teach, or suggest the limitations of "tracking at least one register that is one of loaded from a register file buffer, and written by said second processor, said tracking executed by said second processor," which are contained in amended claim 20.

Tannenbaum is only relied on for asserting that "any instruction executed by hardware can also be executed in software." (Office Action, page 26, paragraph 88). Tannenbaum, however, does not teach, disclose or suggest "tracking at least one register that is one of loaded from a register file buffer, and written by said second processor, said tracking executed by said second processor."

Neither Sundaramoorthy, Tannenbaum, nor the combination of the two, teach, disclose or suggest the limitations contained in Applicant's amended claim 20, as listed above. Since neither Sundaramoorthy, Tannenbaum, nor the combination of the two, teach, disclose or suggest all the limitations of Applicant's amended claim 20, there

would not be any motivation to arrive at Applicant's claimed invention. Thus, Applicant's amended claim 20 is not obvious over Sundaramoorthy in view of Tannenbaum since a *prima facie* case of obviousness has not been met under MPEP §2142. Additionally, the claims that directly or indirectly depend from amended claim 20, namely claims 21-22, 26 and 28, would also not be obvious over Sundaramoorthy in view of Tannenbaum for the same reason.

Accordingly, withdrawal of the 35 U.S.C. § 103(a) rejections for Claims 20-22, 26 and 28 is respectfully requested.

E. It is asserted in the Office Action that claims 23-25 is rejected under 35 U.S.C. §103(a) as being unpatentable over Sundaramoorthy in view of Akkary. Applicant respectfully traverses the aforementioned rejections for the following reasons.

Applicant's claims 23-25 directly or indirectly depend on amended claim 20. As asserted above in section VI and VII(B), neither Sundaramoorthy nor Akkary teach, disclose or suggest the limitations of "tracking at least one register that is one of loaded from a register file buffer, and written by said second processor, said tracking executed by said second processor," which are contained in amended claim 20.

It is asserted in the Office Action that Official Notice is taken that it is well known and expected to set a status bit to indicate the change of state. Applicant agrees. However, how a state is changed and which specific bits are set in order to effect actions is not well known or expected, and much narrower than the broad limitation of setting of a status bit to indicate state. Therefore, Applicant respectfully traverses the Official Notice.

It is asserted in the Office Action that one would be motivated to modify Sundaramoorthy by clearing a store validity bit and setting a mispredicted bit in a load entry in a trace buffer if a replayed store instruction has a matching store ID portion because "the Sundaramoorthy reference does not provide enough detail on how to handle loads and stores..." Applicant respectfully asserts that one would not and could

not be motivated to modify a known system by guessing that the Akkary disclosure would make sense to be added. A similar statement can be made that by adding the disclosure of Akkary to Sundaramoorthy would render Sundaramoorthy useless.

Since neither Sundaramoorthy, Akkary, nor the combination of the two, teach, disclose or suggest all the limitations of Applicant's amended claim 20, there would not be any motivation to arrive at Applicant's claimed invention. Thus, Applicant's amended claim 20 is not obvious over Sundaramoorthy in view of Akkary since a *prima facie* case of obviousness has not been met under MPEP §2142. Additionally, the claims that directly or indirectly depend from amended claim 20, namely claims 23-25, would also not be obvious over Sundaramoorthy in view of Akkary for the same reason.

Accordingly, withdrawal of the 35 U.S.C. § 103(a) rejections for Claims 23-25 is respectfully requested.

F. It is asserted in the Office Action that claim 27 is rejected under 35 U.S.C. §103(a) as being unpatentable over Sundaramoorthy in view of Hennessy and Patterson. Applicant respectfully traverses the aforementioned rejections for the following reasons.

Applicant's claim 27 indirectly depends from Applicant's amended claim 20. As asserted in sections VI and VII(C), Sundaramoorthy does not disclose, teach, or suggest the limitations of "tracking at least one register that is one of loaded from a register file buffer, and written by said second processor, said tracking executed by said second processor," which are contained in amended claim 20.

Hennessy and Patterson are relied upon for disclosing "register renaming is used to reduce name dependencies allowing instructions involved in name dependencies to execute simultaneously or be reordered." (Office Action, page 33, paragraph 123). Hennessy and Patterson does not teach, disclose or suggest "tracking at least one register that is one of loaded from a register file buffer, and written by said second processor, said tracking executed by said second processor."

Moreover, the reason Hennessy and Patterson are relied on is of insignificance to Applicant's claim language. Applicant's claim 27 contains the limitations of "supplying names from the trace buffer to preclude register renaming." Merriam-Webster online dictionary defines the meaning of "preclude" as "to make impossible by necessary consequence : rule out in advance." Therefore, while Applicant is supplying names from the trace buffer, Applicant is doing so to not rename registers. Therefore, Applicant respectfully asserts the Hennessy and Patterson disclosure does not teach, disclose or suggest precluding register renaming.

Neither Sundaramoorthy, Hennessy and Patterson, nor the combination of the two, teach, disclose or suggest the limitations contained in Applicant's amended claim 20 and claim 27, as listed above. Since neither Sundaramoorthy, Hennessy and Patterson, nor the combination of the two, teach, disclose or suggest all the limitations of Applicant's amended claim 20 and claim 27, there would not be any motivation to arrive at Applicant's claimed invention. Thus, Applicant's amended claim 20 and claim 27 are not obvious over Sundaramoorthy in view of Hennessy and Patterson since a *prima facie* case of obviousness has not been met under MPEP §2142.

Accordingly, withdrawal of the 35 U.S.C. § 103(a) rejections for Claim 27 is respectfully requested.

G. It is asserted in the Office Action that claims 29-35 are rejected under 35 U.S.C. §103(a) as being unpatentable over Sundaramoorthy in view of no other prior art. Applicant respectfully traverses the aforementioned rejections for the following reasons.

As asserted above in section VI, Sundaramoorthy does not teach, disclose or suggest the limitations contained in claim 1 of "a first processor and a second processor each having a scoreboard and a decoder."

Since Sundaramoorthy does not teach, disclose or suggest all the limitations of Applicant's amended claim 29, there would not be any motivation to arrive at Applicant's claimed invention. Thus, Applicant's amended claim 29 is not obvious over

Sundaramoorthy in view of no other prior art since a *prima facie* case of obviousness has not been met under MPEP §2142. Additionally, the claims that directly or indirectly depend from amended claim 29, namely claims 30-35, would also not be obvious over Sundaramoorthy in view of no other prior art for the same reason.

Accordingly, withdrawal of the 35 U.S.C. § 103(a) rejections for Claims 29-35 are respectfully requested.

CONCLUSION

In view of the foregoing, it is believed that all claims now pending, namely 1-7 and 9-35, patentably define the subject invention over the prior art of record and are in condition for allowance and such action is earnestly solicited at the earliest possible date.

If necessary, the Commissioner is hereby authorized in this, concurrent and future replies, to charge payment or credit any overpayment to Deposit Account No. 02-2666 for any additional fees required under 37 C.F.R. §§ 1.16 or 1.17, particularly extension of time fees.

Respectfully submitted,

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Dated: July 15, 2004

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CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as First Class Mail with sufficient postage in an envelope addressed to: Mail Stop Amendment, Commissioner for Patents, P. O. Box 1450, Alexandria, Virginia 22313-1450 on July 15, 2004.

Jean Svoboda